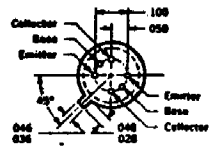
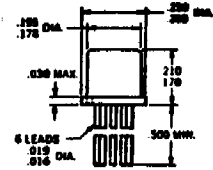


**2N2913 • 2N2914 • 2N2972 • 2N2973**  
 DUAL NPN LOW LEVEL LOW NOISE DIFFERENTIAL AMPLIFIERS  
 DIFFUSED SILICON PLANAR\* TRANSISTORS

- NF ... 4.0 dB (MAX) (2N2913/2N2972)
- V<sub>CEO</sub> ... 45 V (MIN)

**ABSOLUTE MAXIMUM RATINGS (Note 1)**

Maximum Temperatures	-65°C to +200°C			
Storage Temperature	-65°C to +200°C			
Operating Junction Temperature	200°C			
Lead Temperature (80 seconds)	300°C			
Maximum Power Dissipation (Notes 2 & 3)	2N2913 2N2914 One Side	2N2913 2N2914 Both Sides	2N2972 2N2973 One Side	2N2972 2N2973 Both Sides
Total Dissipation				
at 25°C Case Temperature	0.75 W	1.5 W	0.5 W	0.75 W
at 100°C Case Temperature	0.43 W	0.86 W	0.29 W	0.43 W
at 25°C Ambient Temperature	0.3 W	0.5 W	0.25 W	0.30 W
Maximum Voltages and Current				
V <sub>CB0</sub> Collector to Base Voltage	45 V			
V <sub>CEO</sub> Collector to Emitter Voltage (Note 4)	45 V			
V <sub>EBO</sub> Emitter to Base Voltage	6.0 V			
I <sub>C</sub> Collector Current	30 mA			



**CONNECTION DIAGRAM**



NOTES: An dimensions in inches. Leads are gold plated. Package weight - 0.02 gram.

**ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)**

SYMBOL	CHARACTERISTIC	2N2913 2N2972		2N2914 2N2973		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
V <sub>CE(sat)</sub>	Collector Saturation Voltage		0.35		0.35	V	I <sub>C</sub> = 1.0 mA, I <sub>B</sub> = 0.1 mA
I <sub>CBO</sub>	Collector Cutoff Current		10		10	nA	I <sub>E</sub> = 0, V <sub>CB</sub> = 45 V
V <sub>CEO(sus)</sub>	Collector to Emitter Sustaining Voltage (Note 5)	45		45		V	I <sub>E</sub> = 0, V <sub>CB</sub> = 45 V, T <sub>A</sub> = 150°C
NF	Narrow Band Noise Figure		4.0		3.0	dB	I <sub>C</sub> = 10 μA, V <sub>CE</sub> = 5.0 V, f = 1 kHz, R <sub>S</sub> = 10 kΩ, Bandwidth = 200 Hz
NF	Wide Band Noise Figure		4.0		3.0	dB	I <sub>C</sub> = 10 μA, V <sub>CE</sub> = 5.0 V, R <sub>S</sub> = 10 kΩ, f = 10-Hz to 10 kHz, Bandwidth of 15.7 kHz
h <sub>FE</sub>	DC Current Gain	60 150 100 15	240	150 300 225 30	600		I <sub>C</sub> = 10 μA, V <sub>CE</sub> = 5.0 V I <sub>C</sub> = 1.0 mA, V <sub>CE</sub> = 5.0 V I <sub>C</sub> = 100 μA, V <sub>CE</sub> = 5.0 V I <sub>C</sub> = 10 μA, V <sub>CE</sub> = 5.0 V, T <sub>A</sub> = -65°C
V <sub>BE(ON)</sub>	Emitter to Base "On" Voltage		0.7		0.7	V	I <sub>C</sub> = 0.1 mA, V <sub>CE</sub> = 5.0 V
I <sub>CEO</sub>	Collector Cutoff Current		2.0		2.0	nA	I <sub>B</sub> = 0, V <sub>CE</sub> = 5.0 V
I <sub>EBO</sub>	Emitter Cutoff Current		2.0		2.0	nA	I <sub>C</sub> = 0, V <sub>EB</sub> = 5.0 V
h <sub>fe</sub>	High Frequency Current Gain	3.0		3.0			I <sub>C</sub> = 0.5 mA, V <sub>CE</sub> = 5.0 V, f = 20 MHz
C <sub>ob</sub>	Output Capacitance		6.0		6.0	pF	I <sub>E</sub> = 0, V <sub>CB</sub> = 5.0 V, f = 140 kHz
h <sub>ib</sub>	Input Resistance	25	32	25	32	Ω	I <sub>C</sub> = 1.0 mA, V <sub>CE</sub> = 5.0 V, f = 1.0 kHz
h <sub>ob</sub>	Output Conductance		1.0		1.0	μmhos	I <sub>C</sub> = 1.0 mA, V <sub>CB</sub> = 5.0 V, f = 1.0 kHz
BV <sub>CB0</sub>	Collector to Base Breakdown Voltage	45		45		V	I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0
BV <sub>EBO</sub>	Emitter to Base Breakdown Voltage	6.0		6.0		V	I <sub>E</sub> = 10 μA, I <sub>C</sub> = 0

NOTES:  
 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.  
 2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.  
 3. These ratings give a maximum junction temperature of 200°C and junction to ambient thermal resistance of 584°C/W (derating factor of 1.71 mW/°C) for one side; 350°C/W (derating factor of 2.86 mW/°C) for both sides for the 2N2913 and 2N2914. For the 2N2972 and 2N2973, junction to ambient thermal resistance is 700°C/W (derating factor of 1.43 mW/°C) for one side; 584°C/W (derating factor of 1.71 mW/°C) for both sides.  
 4. Rating refers to a high current point where collector to emitter voltage is lowest.  
 5. Pulse conditions: length = 300μs; duty cycle = 1%.  
 6. For product family characteristic curves, refer to Section 5 - 558.  
 \*Planar is a patented Fairchild process.

