

New Jersey Semi-Conductor Products, Inc.

20 STERN AVE.
SPRINGFIELD, NEW JERSEY 07081
U.S.A.

TELEPHONE: (973) 376-2922
(212) 227-6005
FAX: (973) 376-8960

PowerMOS transistor Logic level FET

BUK552-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

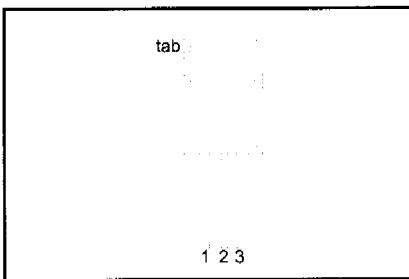
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
V_{DS}	BUK552 Drain-source voltage	-100A 100	-100B 100	V
I_D	Drain current (DC)	10	8.5	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5$ V	0.28	0.35	Ω

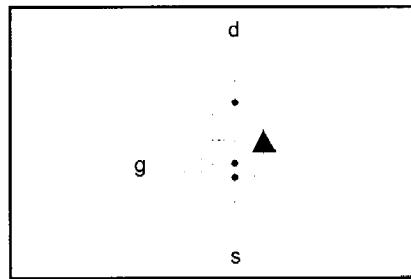
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

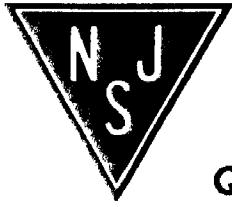
Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS} V_{DGR} $\pm V_{GS}$ $\pm V_{GSM}$	Drain-source voltage	-	-	100		V
	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100		V
	Gate-source voltage	-	-	15		V
	Non-repetitive gate-source voltage	$t_p \leq 50 \mu\text{s}$	-	20		V
I_D I_{D0} I_{DM}	Drain current (DC)	$T_{mb} = 25^\circ\text{C}$	-	-100A	-100B	A
	Drain current (DC)	$T_{mb} = 100^\circ\text{C}$	-	10	8.5	A
	Drain current (pulse peak value)	$T_{mb} = 25^\circ\text{C}$	-	7	6	A
P_{tot} T_{stg} T_j	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	40	34	A
	Storage temperature	-	-55	60		W
	Junction Temperature	-	-	175	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{thj-mb}	Thermal resistance junction to mounting base		-	-	2.5	K/W
R_{thj-a}	Thermal resistance junction to ambient		-	60	-	K/W

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.



STATIC CHARACTERISTICS

$T_{mb} = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V; I_D = 0.25 \text{ mA}$	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	1	10	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125^\circ C$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 15 V; V_{DS} = 0 V$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5 V; I_D = 5.5 \text{ A}$ BUK552-100A $V_{GS} = 5 V; I_D = 5.5 \text{ A}$ BUK552-100B	-	0.25	0.28	Ω
			-	0.3	0.35	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_f	Forward transconductance	$V_{DS} = 25 V; I_D = 5.5 \text{ A}$	4.5	6	-	S
C_{iss}	Input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 \text{ MHz}$	-	400	600	pF
C_{oss}	Output capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 \text{ MHz}$	-	90	120	pF
C_{rss}	Feedback capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 \text{ MHz}$	-	35	50	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30 V; I_D = 3 \text{ A}; V_{GS} = 5 V; R_{GS} = 50 \Omega; R_{gen} = 50 \Omega$	-	12	18	ns
t_r	Turn-on rise time	$V_{DD} = 30 V; I_D = 3 \text{ A}; V_{GS} = 5 V; R_{GS} = 50 \Omega; R_{gen} = 50 \Omega$	-	45	70	ns
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 30 V; I_D = 3 \text{ A}; V_{GS} = 5 V; R_{GS} = 50 \Omega; R_{gen} = 50 \Omega$	-	50	70	ns
t_f	Turn-off fall time	$V_{DD} = 30 V; I_D = 3 \text{ A}; V_{GS} = 5 V; R_{GS} = 50 \Omega; R_{gen} = 50 \Omega$	-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_{mb} = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	10	A
I_{DRM}	Pulsed reverse drain current	-	-	-	40	A
V_{SD}	Diode forward voltage	$I_F = 10 \text{ A}; V_{GS} = 0 V$	-	1.2	1.5	V
t_{rr}	Reverse recovery time	$I_F = 10 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	90	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0 V; V_R = 30 V$	-	0.35	-	μC

AVALANCHE LIMITING VALUE

$T_{mb} = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 10 \text{ A}; V_{DD} \leq 50 V; V_{GS} = 5 V; R_{GS} = 50 \Omega$	-	-	30	mJ

PowerMOS transistor
Logic level FET

BUK552-100A/B

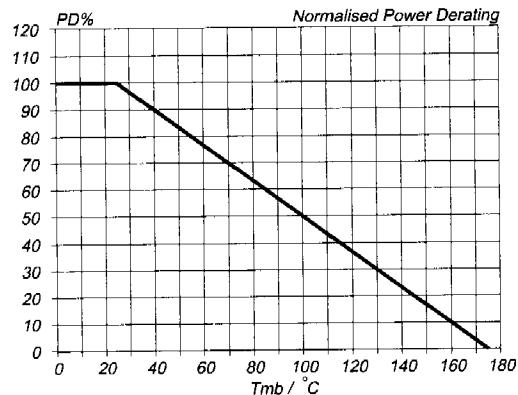


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D, 25^{\circ}\text{C}} = f(T_{mb})$

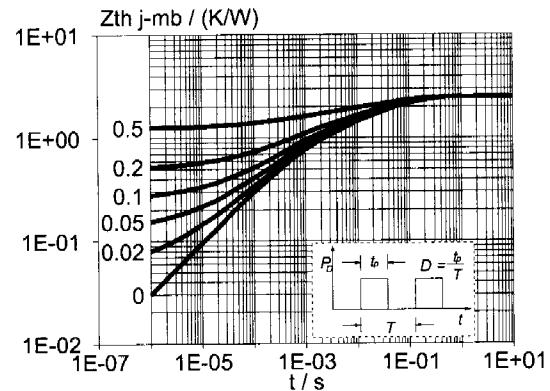


Fig.4. Transient thermal impedance.
 $Z_{th j-mb} = f(t); \text{ parameter } D = t_p/T$

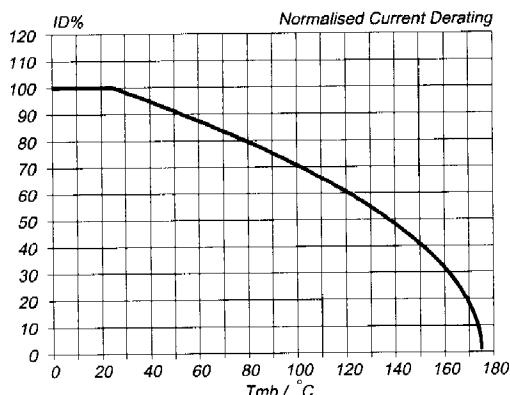


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D, 25^{\circ}\text{C}} = f(T_{mb}); \text{ conditions: } V_{GS} \geq 5 \text{ V}$

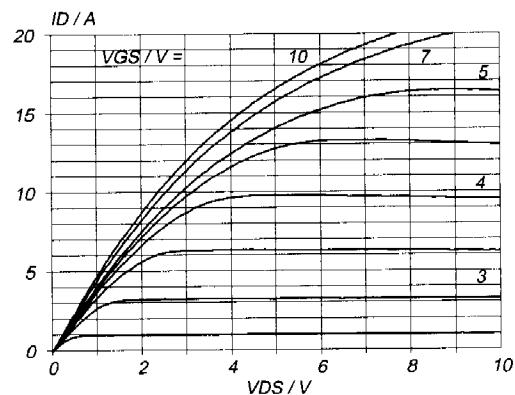


Fig.5. Typical output characteristics, $T_j = 25^{\circ}\text{C}$.
 $I_D = f(V_{DS}); \text{ parameter } V_{GS}$

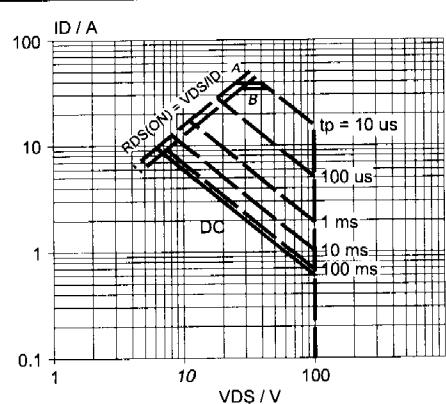


Fig.3. Safe operating area. $T_{mb} = 25^{\circ}\text{C}$
 $I_D \& I_{DM} = f(V_{DS}); I_{DM} \text{ single pulse; parameter } t_p$

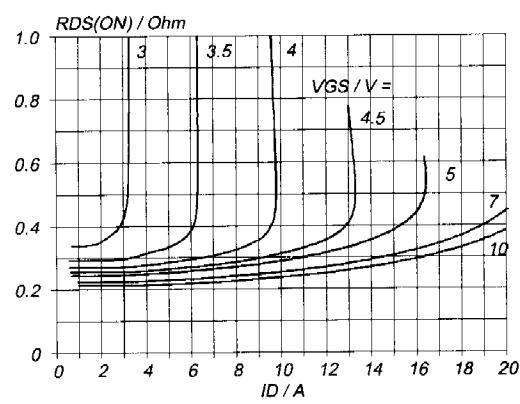


Fig.6. Typical on-state resistance, $T_j = 25^{\circ}\text{C}$.
 $R_{DS(ON)} = f(I_D); \text{ parameter } V_{GS}$

PowerMOS transistor
Logic level FET

BUK552-100A/B

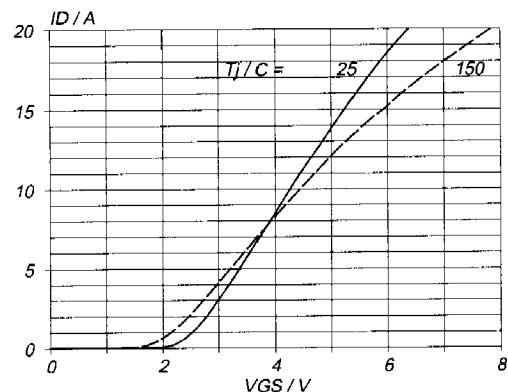


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

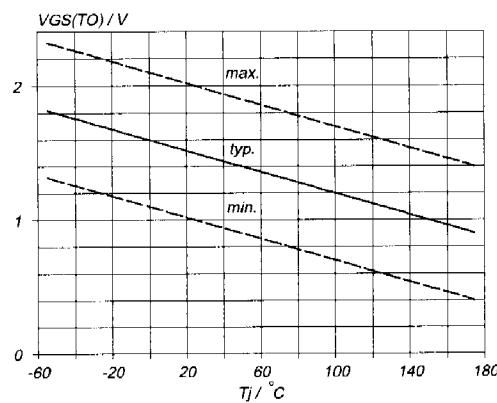


Fig. 10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

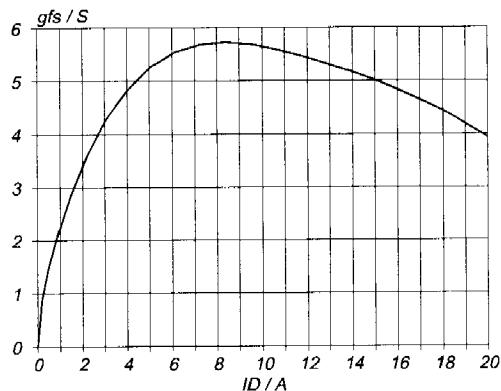


Fig. 8. Typical transconductance, $T_j = 25^\circ\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

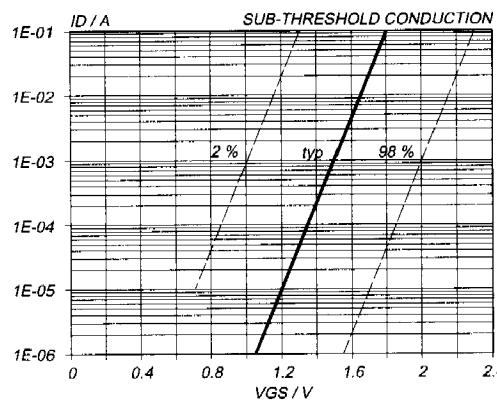


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

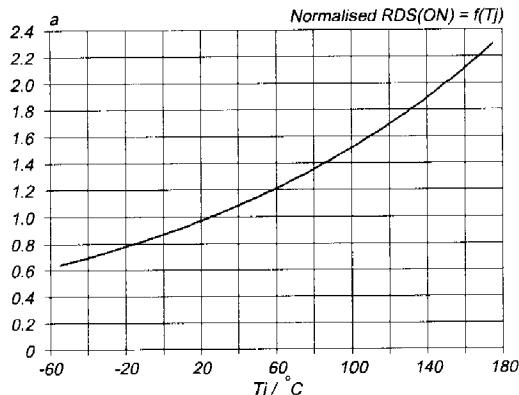


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_j)$; $I_D = 5.5\text{ A}$; $V_{GS} = 5\text{ V}$

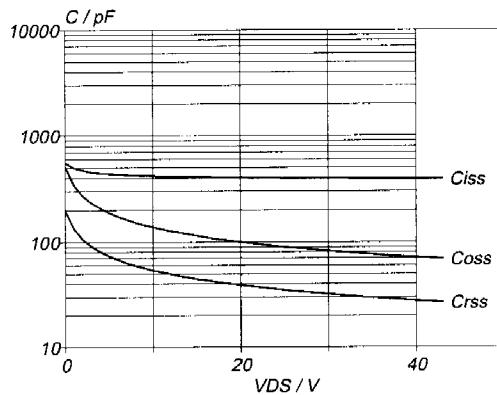


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$