

New Jersey Semi-Conductor Products, Inc.

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GA100, GA101, GA102 Nuclear Radiation Resistant, Planer

Features

- Optimized for Radiation Resistance
- Fully characterized for Worst Case Design
- Post Radiation Design Limits Specified
- Passivated Planar Construction for Maximum Reliability and Parameter Uniformity
- Pulse Currents to 30A
- Max Trigger current 20mA after 3X10 NVT
- Max Holding Current 30mA after 3 X10 NVT

ABSOLUTE MAXIMUM RATINGS

	GA100	GA101	GA102
Repetitive Peak Off-State Voltage, V_{DRM}	30V	60V	80V
D.C. On-State Current, I_T			
75°C Ambient		200mA	
100°C Case		400mA	
Repetitive Peak On-State Current, I_{TRM}		up to 30A	
Surge (non-rep.) On-State Current, I_{TSM} (Sq. Pulse-50ms)		5A	
Peak Gate Current, I_{GM}		250mA	
Average Gate Current, $I_{G(AV)}$		25mA	
Reverse Gate Voltage, V_{GR}		5V	
Reverse Gate Current, I_{GR}		3mA	
Storage Temperature Range		-65°C to +200°C	
Operating Temperature Range		-65°C to +150°C	

MECHANICAL SPECIFICATIONS

	INCHES	MILLIMETERS
A	.178-.195 DIA.	4.52-4.95 DIA.
B	.170-.210	4.31-5.33
C	.5 MIN.	12.70 MIN.
D	.209-.230 DIA.	5.31-5.84 DIA.
E	.017 ± .002 DIA. .001 DIA.	.432 ± .051
F	.020 MAX.	.508 MAX.
G	.100 ± .010 DIA.	2.54 ± .254 DIA.
H	.041 ± .005	1.04 ± .127
J	.028-.048	.711-1.22

TO-18

Quality Semi-Conductors

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	Preradiation Limits			Post 3×10^{14} NVT Design Limits		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
SUBGROUP 1								
Visual and Mechanical	—	—	—	—	—	—	MIL-STD-750 Method 2071	
SUBGROUP 2 (25°C Tests)								
Off-State Current	I_{DRM}	—	.005	0.1	—	1.0	μA	$R_{GK} = 220\Omega$, $V_{DRM} = \text{Rating}$
Reverse Gate Current	I_{GR}	—	.01	0.1	—	1.0	μA	$V_{GR} = 2V$
Input Trigger Current (Note 2)	I_{ST}	1.8	2.3	3.5	—	20	mA	$R_{GK} = 220\Omega$, $V_D = 5V$
Gate Trigger Voltage	V_{GT}	0.4	0.5	0.7	—	1.5	V	$R_{GK} = 220\Omega$, $V_D = 5V$
On-State Voltage	V_T	0.8	1.1	1.5	—	3.0	V	$I_T = 1A$ (pulse test)
Holding Current	I_{H}	0.3	0.7	10	—	30	mA	$R_{GK} = 220\Omega$
SUBGROUP 3 (25°C Tests)								
Off-State Voltage-Critical Rate of Rise	dv_c/dt	20	40	—	—	—	V/ μS	$R_{GK} = 220\Omega$, $V_D = 30V$
Gate Trigger-on Pulse Width	$t_{pg}(\text{on})$	—	.02	.05	—	0.1	μS	$I_G = 25mA$, $I_T = 1A$, $V_D = 30V$
Delay Time	t_d	—	.02	—	—	—	μS	$I_G = 25mA$, $I_T = 1A$, $V_D = 30V$
Rise Time	t_r	—	.05	—	—	—	μS	$I_G = 25mA$, $I_T = 1A$, $V_D = 30V$
Circuit Commutated Turn-off Time	t_q	—	1.5	2.5	—	1.0	μS	$I_T = 1A$, $i_R = 1A$, $R_{GK} = 220\Omega$
SUBGROUP 4 (125°C Tests)								
High Temp Off-State Current	I_{DRM}	—	10	100	—	100	μA	$R_{GK} = 220\Omega$, $V_{DRM} = \text{Rating}$
High Temp Gate Trigger Voltage	V_{GT}	0.1	.17	—	0.1	—	V	$R_{GK} = 220\Omega$, $V_D = 5V$