

2N6303

APPLICATIONS:

- High-Speed Switching
- Medium-Current Switching
- High-Frequency Amplifiers

FEATURES:

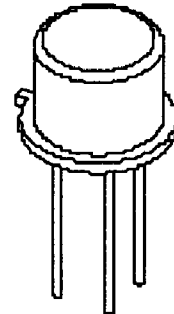
- Collector-Emitter Sustaining Voltage: $V_{CEO(sus)} = -80$ Vdc (Min)
- DC Current Gain: $h_{FE} = 30-150$ @ $I_C = 1.5$ Adc
- Low Collector-Emitter Saturation Voltage:
 $V_{CE(sat)} = -0.75$ Vdc @ $I_C = 1.5$ Adc
- High Current-Gain - Bandwidth Product: $f_T = 90$ MHz (Typ)

Silicon PNP Power Transistors

DESCRIPTION:

These power transistors are produced by PPC's DOUBLE DIFFUSED PLANAR process. This technology produces high voltage devices with excellent switching speeds, frequency response, gain linearity, saturation voltages, high current gain, and safe operating areas. They are intended for use in Commercial, Industrial, and Military power switching, amplifier, and regulator applications.

Ultrasonically bonded leads and controlled die mount techniques are utilized to further increase the SOA capability and inherent reliability of these devices. The temperature range to 200°C permits reliable operation in high ambients, and the hermetically sealed package insures maximum reliability and long life.



TO-5

ABSOLUTE MAXIMUM RATINGS:

SYMBOL	CHARACTERISTIC	VALUE	UNITS
V_{CEO}^*	Collector-Emitter Voltage	- 80	Vdc
V_{CB}^*	Collector-Base Voltage	- 80	Vdc
V_{EB}^*	Emitter-Base Voltage	- 4.0	Vdc
I_C^*	Peak Collector Current	10	Adc
I_C^*	Continuous Collector Current	3.0	Adc
I_B^*	Base Current	0.5	Adc
T_{STG}^*	Storage Temperature	-65 to 200	°C
T_J^*	Operating Junction Temperature	-65 to 200	°C
P_D^*	Total Device Dissipation $T_C = 25^\circ\text{C}$ Derate above 25°C	6.0 34.3	Watts mW/°C
P_D^*	Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	1.0 5.71	Watts mW/°C
θ_{JC}	Thermal Resistance Junction to Case	29	°C/W
	Junction to Ambient	175	°C/W

* Indicates JEDEC registered data.

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ELECTRICAL CHARACTERISTICS:

(25° Case Temperature Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	VALUE		Units
			Min.	Max.	
$V_{CE(sus)}^*$	Collector-Emitter Sustaining Voltage	$I_C = 20 \text{ mAdc}, I_B = 0$ (Note 1)	- 80	----	Vdc
BV_{CBO}^*	Collector-Base Breakdown Voltage	$I_C = 100 \text{ } \mu\text{Adc}, I_E = 0$	- 80	----	Vdc
BV_{EBO}^*	Emitter-Base Breakdown Voltage	$I_E = 100 \text{ } \mu\text{Adc}, I_C = 0$	- 4.0	----	Vdc
I_{CEX}^*	Collector Cutoff Current	$V_{CE} = - 80V, V_{BE(off)} = 2.0 \text{ Vdc}$	----	1.0	μAdc
I_{CBO}^*	Collector Cutoff Current	$V_{CB} = - 80V, I_E = 0, T_C = 150^\circ\text{C}$	----	150	μAdc
h_{FE}^*	DC Current Gain (Note 1)	$I_C = 500 \text{ mAdc}, V_{CE} = - 1.0 \text{ Vdc}$	35	----	----
		$I_C = 1.5 \text{ Adc}, V_{CE} = - 2.0 \text{ Vdc}$	30	150	----
		$I_C = 2.5 \text{ Adc}, V_{CE} = - 3.0 \text{ Vdc}$	20	----	----
		$I_C = 3.0 \text{ Adc}, V_{CE} = - 5.0 \text{ Vdc}$	20	----	----
$V_{CE(sat)}^*$	Collector-Emitter Saturation Voltage (Note 1)	$I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$	----	- 0.5	Vdc
		$I_C = 1.5 \text{ Adc}, I_B = 150 \text{ mAdc}$	----	- 0.75	Vdc
		$I_C = 2.5 \text{ Adc}, I_B = 250 \text{ mAdc}$	----	- 1.3	Vdc
$V_{BE(sat)}^*$	Base-Emitter Saturation Voltage (Note 1)	$I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$	----	- 1.0	Vdc
		$I_C = 1.5 \text{ Adc}, I_B = 150 \text{ mAdc}$	- 0.9	- 1.4	Vdc
		$I_C = 2.5 \text{ Adc}, I_B = 250 \text{ mAdc}$	----	- 2.0	Vdc
f_T^*	Current Gain Bandwidth Product (Note 2)	$I_C = 100 \text{ mAdc}, V_{CE} = - 5.0 \text{ Vdc}, f_{test} = 20 \text{ MHz}$	60	----	MHz
C_{ob}^*	Output Capacitance	$V_{CB} = - 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$	----	120	pF
C_{ib}^*	Input Capacitance	$V_{EB} = - 3.0 \text{ Vdc}, I_C = 0, f = 0.1 \text{ MHz}$	----	1000	pF
td^*	Delay Time	$V_{CC} = - 30 \text{ Vdc}, V_{BE(off)} = 0, I_C = 1.5 \text{ Adc}, I_{B1} = 150 \text{ mAdc}$	----	35	ns
tr^*	Rise Time	$V_{CC} = - 30 \text{ Vdc}, V_{BE(off)} = 0, I_C = 1.5 \text{ Adc}, I_{B1} = 150 \text{ mAdc}$	----	65	ns
ts^*	Storage Time	$V_{CC} = - 30 \text{ Vdc}, I_C = 1.5 \text{ Adc}, I_{B1} = I_{B2} = 150 \text{ mAdc}$	----	325	ns
tf^*	Fall Time	$V_{CC} = - 30 \text{ Vdc}, I_C = 1.5 \text{ Adc}, I_{B1} = I_{B2} = 150 \text{ mAdc}$	----	75	ns

Note 1: Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Note 2: $f_T = |h_{fe}| * f_{test}$

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PACKAGE MECHANICAL DATA:

