

VN0655
VN0660



N-Channel Enhancement-Mode
Vertical DMOS FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package		
			TO-92	TO-220	Die†
550V	20Ω	0.25A	VN0655N3	—	VN0655ND
600V	20Ω	0.25A	VN0660N3	VN0660N5	VN0660ND

†MIL visual screening available

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

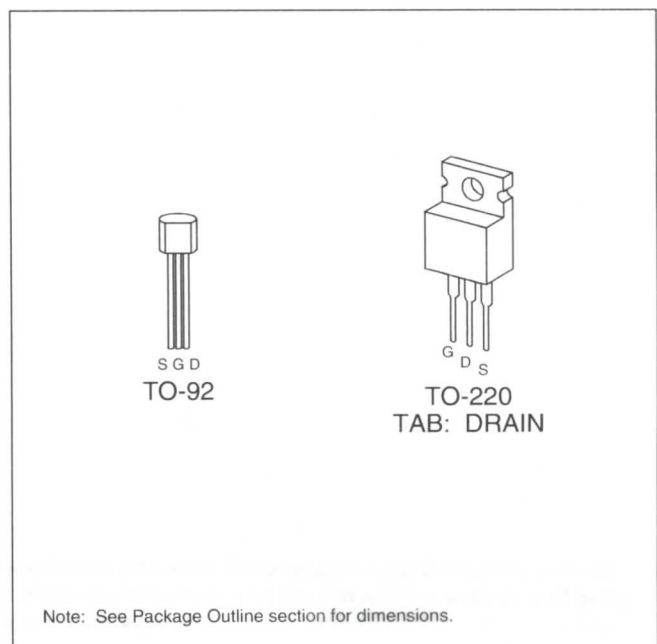
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jC} $^\circ\text{C/W}$	θ_{jA} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-92	0.15A	0.5A	1W	125	170	0.15A	0.5A
TO-220	0.75A	1.5A	45W	5	70	0.75A	1.5A

* I_D (continuous) is limited by max rated T_j .

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0660	600			V $V_{GS} = 0V, I_D = 2mA$
		VN0655	550			
$V_{GS(th)}$	Gate Threshold Voltage	2		4	V	$V_{GS} = V_{DS}, I_D = 2mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 2mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				1	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		0.8		A	$V_{GS} = 5V, V_{DS} = 25V$
		0.25	1.0			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		17		Ω	$V_{GS} = 5V, I_D = 100mA$
			16	20		$V_{GS} = 10V, I_D = 100mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 100mA$
G_{FS}	Forward Transconductance	50	75		mS	$V_{DS} = 25V, I_D = 100mA$
C_{ISS}	Input Capacitance		85	130	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		25	75		
C_{RSS}	Reverse Transfer Capacitance		10	20		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25V,$ $I_D = 0.25A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
t_f	Fall Time			13		
V_{SD}	Diode Forward Voltage Drop			1.8		
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = 100mA$

Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

